WHAT IS CLAIMED IS:

1. A light emitting device comprising a source signal line driver circuit, a first gate signal line driver circuit, a second gate signal line driver circuit, and a pixel portion;

wherein said pixel portion comprises a plurality of pixels;

wherein each of said plurality of pixels comprises an EL element; a first EL driver TFT and a second EL driver TFT for controlling light emitted from said EL element; a switching TFT for controlling said first EL driver TFT and said second EL driver TFT; and an erasure TFT;

wherein said first EL driver TFT and said second EL driver TFT are connected in parallel;

wherein said switching TFT is controlled by said first gate signal line driver circuit;

wherein said erasure TFT is controlled by said second gate signal line driver circuit; and

wherein said EL element is controlled by said switching TFT or the erasure TFT.

2. A light emitting device according to of claim 1, wherein said first EL driver TFT and said second EL driver TFT have the same polarity.

3. A light emitting device according to claim 1, wherein said switching TFT, said erasure TFT, said first EL driver TFT, or said second EL driver TFT is a top gate TFT.

4. A light emitting device according to claim 1, wherein said switching TFT, said erasure TFT, said first EL driver TFT, or said second EL driver TFT is a bottom gate TFT.

5. A light emitting device according to claim 1, wherein said source signal line driver circuit comprises a shift register, a first latch, and a second latch.

6. A light emitting device according to claim 5, wherein said first latch or said second latch comprises two clocked inverters and two inverters.

7. A light emitting device according to claim 1, wherein said first EL driver TFT or said second EL driver TFT is driven in a linear region.

8. A light emitting device according to claim 1, wherein said light emitting device is one of a computer, a video camera, and a DVD player.

9. A light emitting device comprising a source signal line driver circuit, a first gate signal line driver circuit, a second gate signal line driver circuit, and a pixel portion;

wherein said pixel portion comprises a plurality of pixels;

wherein each of said plurality of pixels comprises an EL element; a first EL driver TFT and a second EL driver TFT for controlling light emitted from said EL element; a switching TFT for controlling said first EL driver TFT and said second EL driver TFT; and an erasure TFT;

wherein said first EL driver TFT and said second EL driver TFT are connected in parallel;

wherein said switching TFT is controlled by said first gate signal line driver circuit;

wherein said erasure TFT is controlled by said second gate signal line driver circuit; and

wherein a period during said EL element emits light is controlled by said switching TFTs or said erasure TFTs to perform a gray scale display.

10. A light emitting device comprising a source signal line driver circuit, a first gate signal line driver circuit, a second gate signal line driver circuit, and a pixel portion;

wherein said pixel portion comprises a plurality of pixels;

each of said plurality of pixels comprises an EL element; a switching TFT; an erasure TFT; a first EL driver TFT; and a second driver TFT;

wherein said first EL driver TFT and said second EL driver TFT are connected in parallel;

wherein said switching TFT is controlled by a first gate signal output from said first gate signal line driver circuit;

wherein said erasure TFT is controlled by a second gate signal output from said second gate signal line driver circuit;

wherein said first EL driver TFT and said second EL driver TFT are controlled by said switching TFT or said erasure TFT; and

wherein said EL element is controlled by said first EL driver TFT and said second EL driver TFT.

11. A light emitting device according to of claim 10, wherein said first EL driver TFT and said second EL driver TFT have the same polarity.

12. A light emitting device according to claim 10, wherein said switching TFT, said erasure TFT, said first EL driver TFT, or said second EL driver TFT is a top gate TFT.

13. A light emitting device according to claim 10, wherein said switching TFT, said erasure TFT, said first EL driver TFT, or said second EL driver TFT is a bottom gate TFT.

14. A light emitting device according to claim 10, wherein said source signal line driver circuit comprises a shift register, a first latch, and a second latch.

15. A light emitting device according to claim 14, wherein said first latch or said second latch comprises two clocked inverters and two inverters.

16. A light emitting device according to claim 10, wherein said first EL driver TFT or said second EL driver TFT is driven in a linear region.

17. A light emitting device according to claim 10, wherein said light emitting device is one of a computer, a video camera, and a DVD player.

18. A light emitting device comprising a source signal line driver circuit, a first gate signal line driver circuit, a second gate signal line driver circuit, and a pixel portion;

wherein said pixel portion comprises a plurality of pixels;

each of said plurality of pixels comprises an EL element; a switching TFT; an erasure TFT; a first EL driver TFT; and a second driver TFT;

wherein said first EL driver TFT and said second EL driver TFT are connected in parallel;

wherein said switching TFT is controlled by a first gate signal output from said first gate signal line driver circuit;

wherein said erasure TFT is controlled by a second gate signal output from said second gate signal line driver circuit;

wherein said first EL driver TFT and said second EL driver TFT are controlled by said switching TFT or said erasure TFT; and

wherein a period during which said EL element emits light is controlled by said first EL driver TFT and said second EL driver TFT to perform a gray scale display.

19. A light emitting device comprising: a source signal line driver circuit; a first gate signal line driver circuit; a second gate signal line driver circuit; a pixel portion; a plurality of source signal lines connected to said source signal line driver circuit; a plurality of first gate signal lines connected to said first gate signal line driver circuit; a plurality of second gate signal lines connected to said second gate signal line driver circuit; and a plurality of power source supply lines;

wherein said pixel portion comprises a plurality of pixels;

wherein each of said plurality of pixels comprises a switching TFT; a first EL driver TFT; a second EL driver TFT; an erasure TFT; and an EL element;

wherein said first EL driver TFT and said second EL driver TFT are connected in parallel;

wherein a gate electrode of said switching TFT is connected to one of said plurality of first gate signal lines;

wherein one of a source region and a drain region of the switching TFT is connected to one of said plurality of source signal lines, and the other of said source region and said drain region is connected to a gate electrode of said first EL driver TFT and to a gate electrode of said second EL driver TFT;

wherein a gate electrode of said erasure TFT is connected to one of said plurality of second gate signal lines;

wherein one of a source region and a drain region of said erasure TFT is connected to one of said plurality of power source supply lines, and the other of said source region and said drain region is connected to said gate electrode of said first EL driver TFT and to said gate electrode of said second EL driver TFT;

wherein a source region of said first EL driver TFT and a source region of said second EL driver TFT are connected to said power source supply line; and

wherein a drain region of said first EL driver TFT and a drain region of said second EL driver TFT are connected to said EL element.

20. A light emitting device according to claim 19, wherein said first EL driver TFT and said second EL driver TFT have the same polarity.

21. A light emitting device according to claim 19, wherein said switching TFT, said erasure TFT, said first EL driver TFT, or said second EL driver TFT is a top gate TFT.

22. A light emitting device according to claim 19, wherein said switching TFT, said erasure TFT, said first EL driver TFT, or said second EL driver TFT is a bottom gate TFT.

23. A light emitting device according to claim 19, wherein said source signal line driver circuit comprises a shift register, a first latch, and a second latch.

24. A light emitting device according to claim 19, wherein said first latch or said second latch comprises two clocked inverters and two inverters.

25. A light emitting device according to claim 19, wherein said first EL driver TFT or said second EL driver TFT is driven in a linear region.

26. A light emitting device according to claim 19, wherein said light emitting device is one of a computer, a video camera, and a DVD player.

27. A light emitting device according to claims 19,

wherein said light emitting device comprises a gate wiring connected to said gate electrode of said first EL driver TFT and to said gate electrode of said second EL driver TFT; and a capacitor wiring connected to said power source supply line; and

wherein a gate insulating film of said switching TFT, said erasure TFT, said first EL driver TFT, and said second EL driver TFT is provided between said gate wiring and said capacitor wiring.

28. A light emitting device according claim 19,

wherein, from among said plurality of pixels, two pixels along the direction in which said plurality of first gate signal lines are formed, are adjacent with one of said plurality of power source supply lines therebetween; and

wherein a source region of said first EL driver TFT and a source region of said second EL driver TFT of each of said two pixels are connected to said power source supply line.

29. A light emitting device according to claim 19,

wherein two pixels along the direction in which said plurality of first gate signal lines are formed, are adjacent with one of said plurality of second gate signal lines therebetween;

wherein a gate electrode of said first EL driver TFT and a gate electrode of said second EL driver TFT of each of said two pixels are connected to said plurality of second gate signal line; and

wherein a source region of said first EL driver TFT and a source region of said second EL driver TFT of each of said two pixels are connected to one of said plurality of power source supply lines.

30. A light emitting device according to claim 19, wherein said plurality of first gate signal lines and said plurality of second gate signal lines are formed in parallel.

31. A light emitting device according to claim 30, wherein said plurality of first gate signal lines and said plurality of second gate signal lines overlap with an insulating film therebetween.

32. A light emitting device according to claim 19, wherein said plurality of source signal lines and said plurality of power source supply lines are formed in parallel.

33. A light emitting device according to claim 32, wherein said plurality of source signal lines and the plurality of power source supply lines overlap with an insulating film therebetween.

34. A light emitting device according to claim 19, wherein said plurality of first gate signal lines and said plurality of power source supply lines are formed in parallel.

35. A light emitting device according to claim 34, wherein said plurality of first gate signal lines and said plurality of power source supply lines overlap with an insulating film therebetween.

36. A light emitting device according to claim 19, wherein said plurality of second gate signal lines and said plurality of power source supply lines are formed in parallel.

37. A light emitting device according to claim 36, wherein said plurality of second gate signal lines and said plurality of power source supply lines overlap with an insulating film therebetween.

38. A metod of driving a light emitting device comprising: a source signal line driver circuit; a first gate signal line driver circuit; a second gate signal line driver circuit; a pixel portion; a plurality of source signal lines connected to the source signal line driver circuit; a

plurality of first gate signal lines connected to the first gate signal line driver circuit; a plurality of second gate signal lines connected to the second gate signal line driver circuit; and a plurality of power source supply lines;

wherein said pixel portion comprises a plurality of pixels;

wherein each of said plurality of pixels comprises a switching TFT; a first EL driver TFT; a second EL driver TFT; an erasure TFT; and an EL element;

wherein said first EL driver TFT and said second EL driver TFT are connected in parallel;

wherein a gate electrode of said switching TFT is connected to one of said plurality of first gate signal lines;

wherein one of a source region and a drain region of the switching TFT is connected to one of said plurality of source signal lines, and the other of said source region and said drain region is connected to a gate electrode of said first EL driver TFT and to a gate electrode of said second EL driver TFT;

wherein a gate electrode of said erasure TFT is connected to one of said plurality of second gate signal lines;

wherein one of a source region and a drain region of said erasure TFT is connected to one of said plurality of power source supply lines, and the other of said source region and said drain region is connected to said gate electrode of said first EL driver TFT and to said gate electrode of said second EL driver TFT;

wherein a source region of said first EL driver TFT and a source region of said second EL driver TFT are connected to said power source supply line;

wherein a drain region of said first EL driver TFT and a drain region of said second EL driver TFT are connected to said EL element;

wherein n write in periods Ta1, Ta2, ..., Tan and (m-1) erasure periods Te1, Te2, ..., Te(m-1), ( m is an arbitrary number from 2 to n) are formed within one frame period;

wherein a digital video signal output from said source signal line driver circuit is input to a gate electrode of said first EL driver TFT and to a gate electrode of said second EL driver TFT in said write in periods Ta1, Ta2, ..., Tan;

wherein said digital video signal input to said gate electrode of said first EL driver TFT and to said gate electrode of said second EL driver TFT is erased in said erasure periods Te1, Te2, ..., Te(m-1);

wherein the write in periods Ta1, Ta2, ..., Tam from among said write in periods Ta1, Ta2, ..., Tan, and said erasure periods Te1, Te2, ..., Te(m-1) partly overlap mutually;

wherein periods which begin when said write in periods Ta1, Ta2, ..., Tan begin and finish when the next write in period Ta1, Ta2, ..., Tan begin, or periods which begin when said write in periods Ta1, Ta2, ..., Tan begin and finish said erasure periods Te1, Te2, ..., Te(m-1) begin, are display periods Tr1, Tr2, ..., Trn, respectively;

wherein periods begin when said erasure periods Te1, Te2, ..., Te(m-1) begin and finish when the write in periods after said erasure periods Te1, Te2, ..., Te(m-1) begin, are non-display periods Td1, Td2, ..., Td(m-1), respectively;

wherein it is selected whether said plurality of EL elements emit light or do not emit light in said display periods Tr1, Tr2, ..., Tn in accordance with said digital video signal; and

wherein the ratio of the lengths of said display periods Tr1, Tr2, ..., Trn is expressed by $2^0 : 2^1 : \ldots : 2^{(n-1)}$.

39. A method of said light emitting device according to claim 38, wherein said first EL driver TFT and said second EL driver TFT have the same polarity.

40. A method of said light emitting device according to claim 38, wherein said switching TFT, said erasure TFT, said first EL driver TFT, or said second EL driver TFT is a top gate TFT.

41. A method of said light emitting device according to claim 38, wherein said switching TFT, said erasure TFT, said first EL driver TFT, or said second EL driver TFT is a bottom gate TFT.

42. A method of said light emitting device according to claim 38, wherein said source signal line driver circuit comprises a shift register, a first latch, and a second latch.

43. A method of said light emitting device according to claim 38, wherein said first latch or said second latch comprises two clocked inverters and two inverters.

44. A method of said light emitting device according to claim 38, wherein said first EL driver TFT or said second EL driver TFT is driven in a linear region.

45. A method of said light emitting device according to claim 38, wherein said light emitting device is one of a computer, a video camera, and a DVD player.

46. A method of said light emitting device according to claims 38,

wherein said light emitting device comprises a gate wiring connected to said gate electrode of said first EL driver TFT and to said gate electrode of said second EL driver TFT; and a capacitor wiring connected to said power source supply line; and

wherein a gate insulating film of said switching TFT, said erasure TFT, said first EL driver TFT, and said second EL driver TFT is provided between said gate wiring and said capacitor wiring.

47. A method of said light emitting device according claim 38,

wherein, from among said plurality of pixels, two pixels along the direction in which said plurality of first gate signal lines are formed, are adjacent with one of said plurality of power source supply lines therebetween; and

wherein a source region of said first EL driver TFT and a source region of said second EL driver TFT of each of said two pixels are connected to said power source supply line.

48. A method of said light emitting device according to claim 38,

wherein two pixels along the direction in which said plurality of first gate signal lines are formed, are adjacent with one of said plurality of second gate signal lines therebetween;

wherein a gate electrode of said first EL driver TFT and a gate electrode of said second EL driver TFT of each of said two pixels are connected to said plurality of second gate signal line; and

wherein a source region of said first EL driver TFT and a source region of said second EL driver TFT of each of said two pixels are connected to one of said plurality of power source supply lines.

49. A method of said light emitting device according to claim 38, wherein said plurality of first gate signal lines and said plurality of second gate signal lines are formed in parallel.

50. A method of said light emitting device according to claim 49, wherein said plurality of first gate signal lines and said plurality of second gate signal lines overlap with an insulating film therebetween.

51. A method of said light emitting device according to claim 38, wherein said plurality of source signal lines and said plurality of power source supply lines are formed in parallel.

52. A method of said light emitting device according to claim 51, wherein said plurality of source signal lines and the plurality of power source supply lines overlap with an insulating film therebetween.

53. A method of said light emitting device according to claim 38, wherein said plurality of first gate signal lines and said plurality of power source supply lines are formed in parallel.

54. A method of said light emitting device according to claim 53, wherein said plurality of first gate signal lines and said plurality of power source supply lines overlap with an insulating film therebetween.

55. A method of said light emitting device according to claim 38, wherein said plurality of second gate signal lines and said plurality of power source supply lines are formed in parallel.

56. A method of said light emitting device according to claim 55, wherein said plurality of second gate signal lines and said plurality of power source supply lines overlap with an insulating film therebetween.

57. A method of said light emitting device according to claim 38, wherein the order of appearance of said display periods Tr1, Tr2, ..., Trn is random.

58. A method of said light emitting device according to claim 38, wherein the longest non-display period from among the non-display periods Td1, Td2, ..., Td(m-1) appears last within said frame period.

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59. A methodo of said light emitting device according to claim 38, wherein said write in periods Ta1, Ta2, ..., Tan do not mutually overlap.

60. A method of said light emitting device according to claim 38, wherein said erasure periods Te1, Te2, .... Te(m-1) do not mutually overlap.

61. A light emitting device comprising: a source signal line driver circuit; a first gate signal line driver circuit; a second gate signal line driver circuit; a pixel portion; a plurality of source signal lines connected to the source signal line driver circuit; a plurality of first gate signal lines connected to the first gate signal line driver circuit; a plurality of second gate signal lines connected to the second gate signal line driver circuit; and a plurality of power source supply lines;

wherein said pixel portion comprises a plurality of pixels;

wherein each of said plurality of pixels comprises a switching TFT; a first EL driver TFT; a second EL driver TFT; an erasure TFT; and an EL element;

wherein said first EL driver TFT and said second EL driver TFT are connected in parallel;

wherein said EL element comprises a pixel electrode, an opposing electrode maintained at a constant electric potential, and an EL layer provided between said pixel electrode and said opposing electrode;

wherein a gate electrode of said switching TFT is connected to one of said plurality of first gate signal lines;

wherein one of a source region and a drain region of the switching TFT is connected to one of said plurality of source signal lines, and the other of said source region and said drain region is connected to a gate electrode of said first EL driver TFT and to a gate electrode of said second EL driver TFT;

wherein a gate electrode of said erasure TFT is connected to one of said plurality of second gate signal lines;

wherein one of a source region and a drain region of said erasure TFT is connected to one of said plurality of power source supply lines, and the other of said source

region and said drain region is connected to said gate electrode of said first EL driver TFT and to said gate electrode of said second EL driver TFT;

wherein a source region of said first EL driver TFT and a source region of said second EL driver TFT are connected to said power source supply line; and

wherein a drain region of said first EL driver TFT and a drain region of said second EL driver TFT are connected to said pixel electrode of said EL element.

62. A light emitting device according to claim 61, wherein said EL layer is formed of a low-molecular organic material or a polymer organic material.

63. A light emitting device according to claim 61, wherein said low-molecular organic material is made of $Alq_3$ (tris-8-quinolilite-aluminium) or TPD (triphenylamine derivative).

64. A light emitting device according to claim 61, wherein said polymer organic material is made of PPV (polyphenylene vinylene), PVK (polyvinylcarbazole) or polycarbonate.

65. A light emitting device according to claim 61, wherein said first EL driver TFT and said second EL driver TFT are p-channel TFTs when said pixel electrode is an anode.

66. A light emitting device according to claim 61, wherein said first EL driver TFT and said second EL driver TFT are n-channel TFTs when said pixel electrode is a cathode.

67. A light emitting device according to claim 61,

wherein said pixel electrode and said drain region of said first EL driver TFT, and said pixel electrode and said drain region of said second EL driver TFT are connected through at least one wiring; and

wherein a bank is formed on a region where said pixel electrode is connected to at least said one wiring.

68. A light emitting device according to claim 61, wherein said bank has a light shielding property.

69. Amethod of driving a light emitting device comprising: a source signal line driver circuit; a first gate signal line driver circuit; a second gate signal line driver circuit; a pixel portion; a plurality of source signal lines connected to the source signal line driver circuit; a plurality of first gate signal lines connected to the first gate signal line driver circuit; a plurality of second gate signal lines connected to the second gate signal line driver circuit; and a plurality of power source supply lines;

wherein said pixel portion comprises a plurality of pixels;

wherein each of said plurality of pixels comprises a switching TFT; a first EL driver TFT; a second EL driver TFT; an erasure TFT; and an EL element;

wherein said first EL driver TFT and said second EL driver TFT are connected in parallel;

wherein said EL element comprises a pixel electrode, an opposing electrode maintained at a constant electric potential, and an EL layer provided between said pixel electrode and said opposing electrode;

wherein a gate electrode of said switching TFT is connected to one of said plurality of first gate signal lines;

wherein one of a source region and a drain region of the switching TFT is connected to one of said plurality of source signal lines, and the other of said source region and said drain region is connected to a gate electrode of said first EL driver TFT and to a gate electrode of said second EL driver TFT;

wherein a gate electrode of said erasure TFT is connected to one of said plurality of second gate signal lines;

wherein one of a source region and a drain region of said erasure TFT is connected to one of said plurality of power source supply lines, and the other of said source region and said drain region is connected to said gate electrode of said first EL driver TFT and to said gate electrode of said second EL driver TFT;

wherein a source region of said first EL driver TFT and a source region of said second EL driver TFT are connected to said power source supply line;

wherein a drain region of said first EL driver TFT and a drain region of said second EL driver TFT are connected to said pixel electrode of said EL element;

wherein n write in periods Ta1, Ta2, ..., Tan and (m-1) erasure periods Te1, Te2, ..., Te(m-1), ( m is an arbitrary number from 2 to n) are formed within one frame period;

wherein a digital video signal output from said source signal line driver circuit is input to a gate electrode of said first EL driver TFT and to a gate electrode of said second EL driver TFT in said write in periods Ta1, Ta2, ..., Tan;

wherein said digital video signal input to said gate electrode of said first EL driver TFT and to said gate electrode of said second EL driver TFT is erased in said erasure periods Te1, Te2, ..., Te(m-1);

wherein the write in periods Ta1, Ta2, ..., Tam from among said write in periods Ta1, Ta2, ..., Tan, and said erasure periods Te1, Te2, ..., Te(m-1) partly overlap mutually;

wherein periods which begin when said write in periods Ta1, Ta2, ..., Tan begin and finish when the next write in period Ta1, Ta2, ..., Tan begin, or periods which begin when said write in periods Ta1, Ta2, ..., Tan begin and finish said erasure periods Te1, Te2, ..., Te(m-1) begin, are display periods Tr1, Tr2, ..., Trn, respectively;

wherein periods begin when said erasure periods Te1, Te2, ..., Te(m-1) begin and finish when the write in periods after said erasure periods Te1, Te2, ..., Te(m-1) begin, are non-display periods Td1, Td2, ..., Td(m-1), respectively;

wherein it is selected whether said plurality of EL elements emit light or do not emit light in said display periods Tr1, Tr2, ..., Tn in accordance with said digital video signal; and

wherein the ratio of the lengths of said display periods Tr1, Tr2, ..., Trn is expressed by $2^0 : 2^1 : \ldots : 2^{(n-1)}$.

70. A method of said light emitting device according to claim 69, wherein said EL layer is formed of a low-molecular organic material or a polymer organic material.

71. A method of said light emitting device according to claim 69, wherein said low-molecular organic material is made of $Alq_3$ (tris-8-quinolilite-aluminium) or TPD (triphenylamine derivative).

72. A method of said light emitting device according to claim 69, wherein said polymer organic material is made of PPV (polyphenylene vinylene), PVK (polyvinylcarbazole) or polycarbonate.

73. A method of said light emitting device according to claim 69, wherein said first EL driver TFT and said second EL driver TFT are p-channel TFTs when said pixel electrode is an anode.

74. A method of said light emitting device according to claim 69, wherein said first EL driver TFT and said second EL driver TFT are n-channel TFTs when said pixel electrode is a cathode.

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75. A method of said light emitting device according to claim 69,

wherein said pixel electrode and said drain region of said first EL driver TFT, and said pixel electrode and said drain region of said second EL driver TFT are connected through at least one wiring; and

wherein a bank is formed on a region where said pixel electrode said is connected to said at least one wiring.

76. A light emitting device comprising a plurality of pixels, each of said plurality of pixels comprising a source signal line; a first gate signal line; a second gate signal line; an power source supply line; a switching TFT; a first EL driver TFT; a second EL driver TFT; an erasure TFT; and an EL element;

wherein a gate electrode of said switching TFT is connected to the first gate signal line;

wherein one of a source region and a drain region of said switching TFT is connected to said source signal line, and the other of one of said source region and said drain region is connected to a gate electrode of said first EL driver TFT and to a gate electrode of said second EL driver TFT;

wherein said first EL driver TFT and said second EL driver TFT are connected in parallel;

wherein a gate electrode of said erasure TFT is connected to said second gate signal line;

wherein one of a source region and a drain region of said erasure TFT is connected to said power source supply line, and the other of one of said source region and said drain region is connected to said gate electrode of said first EL driver TFT and said gate electrode of said second EL driver TFT;

wherein a source region of said first EL driver TFT and a source region of said second EL driver TFT are connected to said power source supply line; and

wherein a drain region of said first EL driver TFT and a drain region of said second EL driver TFT are connected to said EL element.

77. A light emitting device according to claim 76, wherein said light emitting device is one of a computer, a video camera, and a DVD player.

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